REMARKS

In the Office Action of April 12, 2007, the Examiner (1) objected to the specification; (2) rejected claims 1-3, 7, 9-10, 12, 21, and 24 as allegedly anticipated by U.S. Patent No. 6,766,460 ("Evoy"); (3) rejected claims 15 and 18 as allegedly anticipated by U.S. Patent No. 5,596,759 ("Miller"); and (4) rejected claims 4-5, 13-14, and 22-23 as allegedly obvious over Evoy in view of U.S. Patent No. 4,565,404 ("Shenk"); (5) rejected claims 6, 11, and 25 as allegedly obvious over Evoy in view of U.S. Patent No. 6,678,830 ("Mustafa"); (6) rejected claim 8 as allegedly obvious over Evoy in view of U.S. Patent No. 4,420,806 ("Johnson"); (7) rejected claims 16-17 as allegedly obvious over Miller in view of Shenk; (8) rejected claim 19 as allegedly obvious over Miller in view of Johnson; and (9) rejected claim 20 as allegedly obvious over Miller in view of Mustafa.

With this response, Applicants amend claim 15. Applicants believe that pending claims are allowable over the art of record and respectfully request reconsideration.

I. AMENDMENTS TO THE SPECIFICATION

With respect to paragraph [0001], Applicants hereby update the list of cross-referenced applications with the serial numbers.

II. ART BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly anticipated by Evoy (U.S. Patent No.6,766,460)

Evoy is directed to a power management system in a Java accelerator environment. (Evoy Title). In particular, Evoy appears to disclose a power management system between a host processor and a Java processor. (Evoy Abstract). Evoy teaches that the host processor generates a Java mode signal which informs the power management system that a Java application needs to be executed by the Java processor. (Evoy Col. 6, lines 15-22). Upon receiving the signal the power management system lowers the voltage on the host processor and increases the voltage on the Java processor. (Evoy Col. 6, lines 23-31). Thus, Evoy appears to disclose a power management system initiated by generating a signal at the host processor, but is silent as to how the determination that a Java application needs to be executed.

Claim 1, by contrast, specifically recites, "a first processor that executes a transaction targeting a pre-determined address….a wait unit coupled to said first and second processor, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode." Applicants respectfully submit that Evoy does not expressly or inherently teach such a system. Although Evoy may enter a reduced power state, the trigger for entering that reduced power state is the determination that a Java application needs to be executed; however, Evoy is silent as to how the determination is made. Thus, Evoy fails to expressly or inherently teach "a wait unit coupled to said first and second processor, **said wait unit detects said pre-determined address** and asserts a wait signal to cause said first processor to enter a wait mode."

Moreover, in Evoy the host processor makes the determination that a Java application needs to be executed. Thus, Evoy further fails to expressly or inherently teach a "**wait unit [that] detects** said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode."

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-8), should be allowed.

B. Claim 9

Claim 9 stands rejected as allegedly anticipated by Evoy (U.S. Patent No. 6,766,460.

Evoy is directed to a power management system in a Java accelerator environment (Evoy title). In particular, Evoy teaches a power management system between two processors, where the power management is initiated after the host processor generates a signal (abstract).

Claim 9, by contrast, specifically recites, "detecting the transaction to said pre-determined address; asserting a wait signal upon detection to the transaction to cause a processor to stall." Applicants respectfully submit that Evoy does not expressly or inherently teach such a system. Although Evoy may enter a reduced power state, the trigger for entering that reduced power state is the determination that a Java application needs to be executed; however, Evoy is silent as to how the determination is made. Further, the host processor makes the determination that a Java application needs to be executed. Thus, Evoy fails to expressly or inherently teach

"**detecting the transaction to said pre-determined address; asserting a wait signal** upon detection to the transaction to cause a processor to stall."

Based on the foregoing, Applicants respectfully submit that claim 9, and all claims which depend from claim 9 (claims 10-14), should be allowed.

C. Claim 15

Claim 15 stands rejected as allegedly anticipated by Miller (U.S. Patent No. 5,596,759). Applicants amend claim 15 to make more clear the first processor is to stall, and not to define over any prior art.

Miller is directed to initializing a multiple processor computer system using a common ROM. In particular, Miller appears to disclose a primary processor which is active during power up, and a secondary processor which is kept in held a state during power up. (Miller Col. 5, lines 35-40). Miller teaches that the secondary processor is activated by either clearing a reset bit or a sleep bit. (Miller Col. 5, lines 42-61). Specifically, the primary processor activates the secondary processor by clearing the sleep bit. (Miller Col. 10, lines 19-23). The Office action states that "once the second processor is activated then the first processor waits for completion signal from processor." However, upon closer examination of Miller, it appears that the first processor does not wait for completion signal; instead it continues the execution of its on code. (Miller Col. 10, lines 39-45). Thus, Miller teaches that the primary processor continues to operate after clearing the sleep bit on the secondary processor.

Claim 15, by contrast, specifically recites "a decode logic unit that determines when a first processor runs a transaction to a pre-determined address…wherein said logic asserts a signal propagated by the first processor interface to cause said **first** processor to stall." Applicants respectfully submit that Miller does not expressly or inherently teach such a unit. Miller teaches a primary processor activating a secondary processor, but continuing to execute its own code after the activation. Thus, Miller fails to expressly or inherently teach "a decode logic unit that determines when a first processor runs a transaction to a pre-determined address…wherein said logic asserts a signal propagated by the first processor interface to cause said **first** processor to stall."

Based on the foregoing, Applicants respectfully submit that claim 15, and all claims which depend from claim 15 (claims 16-20), should be allowed.

D. Claim 21

Claim 21 stands rejected as allegedly anticipated by Evoy (U.S. Patent No. 6,766,460)

Evoy is directed to a power management system in a Java accelerator environment. (Evoy Title). In particular, Evoy teaches a power management system between two processors, where the power management is initiated after the host processor generates a signal. (Evoy Abstract).

Claim 21, by contrast, specifically recites, "means for detecting a transaction targeting a pre-determined address and for asserting a wait signal to said processor to cause the first processor to enter a wait state." Applicants respectfully submit that Evoy does not expressly or inherently teach such a system. Although Evoy may enter a reduced power state, the trigger for entering that reduced power state is the determination that a Java application needs to be executed; however, Evoy is silent as to how the determination is made. Further, the host processor makes the determination that a Java application needs to be executed. Thus, Evoy fails to expressly or inherently teach "means for **detecting a transaction targeting a pre-determined address and for asserting a wait signal** to said processor to cause the first processor to enter a wait state."

Based on the foregoing, Applicants respectfully submit that claim 21, and all claims which depend from claim 21 (claims 22-25), should be allowed.

III. CONCLUSION

In course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

/Utpal D. Shah/

Utpal D. Shah
PTO Reg. No. 60,047
CONLEY ROSE, P.C.
(512) 391-1900 (Phone)
(512) 320-9182 (Fax)
AGENT FOR APPLICANTS